

REMARKS

By this Amendment, Applicants amend claims 1-11 to more appropriately define the invention and add new claims 12-16 to protect additional aspects thereof. Claims 1-16 are therefore pending.

In the Office Action of January 5, 2004¹ ("OA"), claims 1-11 were rejected under the so called "judicially created doctrine of double patenting" over claims 1-27 of U.S. Patent No. 6,449,750 to Tsuchiya ("*Tsuchiya '750*"); rejected under 35 U.S.C. § 112, first paragraph, for "failing to comply with the written description requirement;" and also rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In addition, claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,912,819 to *Kucukcakar et al.* ("*Kucukcakar*"); claims 2-11 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,805,861 to *Gilbert et al.* ("*Gilbert*"); claims 1-4, and 8 were objected to for informalities; and the drawings were objected to under 37 C.F.R. § 1.83(a). Applicants address the rejections and objections as set forth below.

Regarding the Drawings

The Examiner indicated that corrected drawings are required because the term "CONE" is misspelled as "CORN" in the Figures (OA at 2). The Examiner also objected to the drawings under 37 C.F.R. § 1.83(a), requiring that "[t]he drawings must show every feature of the invention specified in the claims" (OA at 2).

In response, Applicants file herewith four (4) sheets of replacement drawings, each labeled "Replacement Sheet," containing Figs. 1, 2, 4A, 4B, 5A, and 5B. In the replacement

¹ The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether or not any such statement is identified herein, Applicants decline to automatically subscribe to any statement or characterization in the Office Action.

drawings, Figures 1, 2, 4A, 4B, 5A, and 5B denote the term “CONE” instead of “CORN.” In addition, Applicants amend Figure 2 so that item S102 reads “DIVIDE CIRCUIT DESCRIPTION INTO LOGIC CONES.” Applicants submit that no new matter is introduced by the amendments to the drawings. Applicants deem the Examiner’s objection to the drawings overcome².

Applicants request that the replacement drawings be made of official record in the above-identified patent application. If the drawings for any reason are not in full compliance with the pertinent statutes and regulations, please so advise the undersigned.

Objection to claims 1-4 and 8

The Examiner rejected claims 1-4 and 8 because of informalities, alleging that the claim language “‘and others not’ is not a suitable description for separation between operations” (OA at 3). By this amendment, Applicants amend claims 1-4 and 8 to, among other things, address the alleged informality. Applicants deem the objection to claims 1-4 and 8 overcome.

Regarding the double patenting rejection of claims 1-11

In the Office Action, the Examiner rejected claims 1-11 under the so called “judicially created doctrine of double patenting” over claims 1-27 of *Tsuchiya* ‘750. According to the Examiner:

The subject matter in the instant application is fully disclosed in [*Tsuchiya* ‘750] ... and is covered by the patent since the patent and the application are claiming common subject matter....

Applicants traverse this rejection for the following reasons.

Initially, Applicants point out that the double patenting rejection set forth in the Office Action is ambiguous. Applicants call attention to M.P.E.P. § 804, which states:

² The Examiner alleged that the term “predetermined unit” has been frequently used in [the] claims ... [b]ut there is no recitation for the generation of “logic cone” (OA at 3). Claims 1-11, however, do not recite a “predetermined unit,” as currently presented.

There are generally two types of double patenting rejections. One is the “same invention” type double patenting rejection based on 35 U.S.C. 101 which states in the singular that an inventor “may obtain a patent”. The second is the “nonstatutory-type” double patenting rejection based on a judicially created doctrine grounded in public policy and which is primarily intended to prevent prolongation of the patent term by prohibiting claims in a second patent not patentably distinguishing from claims in a first patent. Nonstatutory double patenting includes rejections based on one-way determination of obviousness and on two-way determination of obviousness....

While indicating that the rejection of claims 1-11 is nonstatutory and “based on a judicially created doctrine grounded in public policy...” (OA at 4), the Office Action does not clearly articulate whether the rejection is an “obviousness” type double patenting rejection. Notwithstanding this ambiguity, Applicants treat the rejection as if it were of the usual obviousness type. Applicants, nevertheless, request clarification in the next Action as to the basis for rejection.

Further, the following statement in the Office Action is ambiguous:

Consider, for example, claim 4 of [*Tsuchiya* ‘750] ... as compared to application claim 1... “[t]he only difference appears to be that claim 1 of [*Tsuchiya* ‘750] ... recited more detail.

Applicants cannot discern whether the Examiner is relying on claim 1 or 4 of *Tsuchiya* ‘750 as the basis for rejection. While apparently comparing claim 4 of *Tsuchiya* ‘750 to claim 1 of the present application, the Examiner relies on the recitations of claim 1 of *Tsuchiya* ‘750. The above ambiguity notwithstanding, Applicants submit that claims 1-11, as currently presented, are not “fully disclosed” in *Tsuchiya* ‘750.

Tsuchiya ‘750 fails to disclose “a logic verification unit configured to perform a logic verification by using a circuit description defining structure and specification of a circuit to be designed and a plurality of test vectors,” as recited in independent claim 1. *Tsuchiya* ‘750 further

fails to disclose “a profile information generating unit configured to store information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as a profile information,” as claimed. Moreover, *Tsuchiya* ‘750 does not disclose the “test vector classifying unit” recited in claim 1.

Regarding independent claim 3, *Tsuchiya* ‘750 fails to disclose the claimed “performing a logic verification....” *Tsuchiya* ‘750 further fails to disclose the claimed “storing” and “classifying” elements of claim 3. Regarding independent claim 8, *Tsuchiya* ‘750 fails to disclose instructions configured to “perform a logic verification,” “store information,” or “classify,” as recited in the claim.

Claims 2, 4-7, and 9-11 depend from claims 1, 3, and 8, respectively, and therefore include all of the elements recited in base claims 1, 3, and 8. Because *Tsuchiya* ‘750 does not disclose all of the elements of base claims 1, 3, and 8, *Tsuchiya* ‘750 also fails to disclose all of the elements of dependent claims 2, 4-7, and 9-11.

In view of the above-noted differences between the claimed subject matter in the present application and *Tsuchiya* ‘750, Applicants submit that a rejection based on non-statutory double patenting is improper. In other words, Applicants submit that the claims in *Tsuchiya* ‘750 are patentably distinct from the claims of the instant application. Applicants therefore request withdrawal of the non-statutory double patenting rejection of claims 1-11.

Rejections under 35 U.S.C. § 112

The Examiner rejected claims 1-11 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. In particular, the Examiner alleged that “[t]he phrase ‘predetermined unit’ ... has not been defined in the specification” (OA at 6).

The Examiner also rejected claims 1-11 under 35 U.S.C. § 112, second paragraph, as being indefinite. The Examiner alleges that “[t]he phrase ‘predetermined unit’ is ambiguous”

(OA at 7). Claims 1-11, as currently presented, do not recite a “predetermined unit” and are fully compliant with 35 U.S.C. § 112, first and second paragraphs³. Applicants therefore request withdrawal of the rejection of claims 1-11 under 35 U.S.C. § 112, first and second paragraphs.

Regarding the Examiner’s Claim Interpretation

Applicants do not acquiesce to the Examiner’s “interpretations” of various claim terms (OA at 7-8). In fact, Applicants point out the terms “corn,” “logic cone unit,” and “predetermined unit” are not recited in the claims as currently presented. Further, Applicants point out that the term “logic cone” is described in the specification (see e.g., page 8)⁴. Applicants also submit that claim 2, for example, does in fact recite appropriate function for the claimed “formal verification unit.” In addition, Applicants note that claim 2, as currently presented, recites “a logic cone dividing unit,” and claim 4 recites “dividing the circuit description into the logic cones.”

Rejection of claim 1 under 35 U.S.C. § 102(e)

Applicants traverse the rejection of claim 1 under 35 U.S.C. § 102(e) based on *Kucukcakar* because the reference fails to anticipate the claim. In order to properly anticipate Applicants’ claimed invention under 35 U.S.C. § 102(e), each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Further, “[t]he identical invention must be shown in as complete detail as is contained in the...claim.” See M.P.E.P. § 2131 (8th Ed., Aug. 2001), quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Finally, “[t]he elements must be arranged as required by the claim.” M.P.E.P. § 2131 (8th Ed. 2001), p.

³ Although Applicants amend the claims, Applicants do not acquiesce to the allegations in the Office Action regarding the alleged “failure to comply with the written description requirement” and indefinites of the claims.

2100-69. *Kucukcakar* does not teach each and every element recited in Applicants' claims, as required.

Independent claim 1, as currently presented, recites a combination of elements including:

a logic verification unit configured to perform a logic verification by using a circuit description defining structure and specification of a circuit to be designed and a plurality of test vectors;

a profile information generating unit configured to store information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as a profile information;

a logic cone specifying unit configured to specify changed logic cones of a changed circuit description automatically; and

a test vector classifying unit configured to classify the test vectors into test vectors related to the changed logic cones and test vectors unrelated to the changed logic cones by using the profile information.

Kucukcakar is directed to “a computer implemented architectural design method for designing an integrated circuit” (Abstract). As noted by the Examiner, *Kucukcakar* mentions that “[t]he designer identifies the modified portion interactively and completes the modified RTL implementation by interactively branching to other steps in any order to perform design tasks on only the modified portion” (Col. 9, lines 62-65; OA at 9). *Kucukcakar*, however, does not teach at least the claimed “logic verification unit” and “profile information generating unit.” Moreover, *Kucukcakar* fails to disclose the “logic cone specifying unit” and “test vector classifying unit,” as currently recited in claim 1. *Kucukcakar*, thus, does not teach each and every feature recited in claim 1.

⁴ In referring to the specification above, Applicants do not intend to limit the scope of the claims to the exemplary embodiments shown in the drawings and described in the specification. Rather, Applicants expressly affirm their entitlement to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law.

As set forth above, anticipation under 35 U.S.C. § 102(e) requires that each and every claim element be disclosed in as complete detail as is in the claim by the applied reference.

Kucukcakar does not teach each and every feature of independent claim 1 and thus, as a matter of law, cannot anticipate claim 1. The rejection of independent claim 1 under 35 U.S.C. §102(e) as anticipated by *Kucukcakar* should therefore be withdrawn. Accordingly, Applicants request withdrawal of the rejection of claim 1 under 35 U.S.C. §102(e) and the timely allowance of this pending claim.

Rejection of claims 2-11 under 35 U.S.C. § 102(e)

Applicants traverse the rejection of claims 2-11 under 35 U.S.C. § 102(e) based on *Gilbert* because *Gilbert* fails to anticipate the claims.

Independent claim 3 recites a method including, inter alia:

storing information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as profile information...and

classifying the test vectors into test vectors related to the changed logic cones and test vectors unrelated to the changed logic cones by using the profile information.

Gilbert fails to teach the above claimed elements. As noted by the Examiner, *Gilbert* mentions storing a “gate level description ... in a design database” (col. 4, lines 46-47; OA at 10). *Gilbert*, however, does not teach at least “storing information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as profile information,” as claimed. Moreover, although (as noted by the Examiner) *Gilbert* mentions “component and net names from ... [a] selected cone of logic,” the reference does not teach at least “classifying ... test vectors into test vectors related to the changed logic cones and test vectors unrelated to the changed logic cones by using the profile information,” as

claimed (col. 5, lines 2-3; OA at 10-11). *Gilbert* does not teach each and every feature recited in claim 3 and, therefore, cannot anticipate claim 3.

Independent claims 8, although of different scope, includes recitations similar to the recitations in claim 3 discussed above. In particular, claim 8 recites, *inter alia*:

instructions configured to store information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as profile information ... and

instructions configured to classify the test vectors into test vectors related to logic cones the changed and test vectors unrelated to the changed logic cones by using the profile information.

For at least the reasons presented above in connection with claim 3, independent claim 8 is not anticipated by *Gilbert*.

Because *Gilbert* fails to anticipate independent claims 3 and 8, the rejection of these claims under 35 U.S.C. § 102(e) based on *Gilbert* should be withdrawn. The rejection of claims 4-7 and 9-11 should be withdrawn as well, at least because of the respective dependence of those claims from base claims 3 and 8.

Claim 2 depends from claim 1 and should be allowed by virtue of such dependence. Moreover, Applicants submit that *Gilbert* does not teach each and every element recited in claim 1 and therefore required by claim 2.

Accordingly, Applicants request withdrawal of the rejection of claims 2-11 under 35 U.S.C. §102(e) and the timely allowance of these pending claims.

New claims

New claims 12-14 depend from base claim 1, new claim 15 depends from base claim 3, and new claim 16 depends from base claim 8. Claims 12-16 should be allowed for at least the same reasons as presented above in connection with base claims 1, 3, and 8.

Conclusion


In view of the foregoing, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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Dated: April 5, 2004

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